5. The semiconductor device of claim 1, wherein
the first gate separation pattern is on the device isolation layer; and
a bottom surface of the first gate separation pattern is at a lower level than a topmost surface of the device isolation layer.

6. The semiconductor device of claim 1, wherein a top surface of the first gate separation pattern is at the same level as a top surface of the gate electrode.

7. The semiconductor device of claim 1, wherein the first gate separation pattern extends in the first direction.

8. The semiconductor device of claim 1, further comprising:
a second gate separation pattern dividing the gate electrode into segments spaced apart from each other in the second direction,
wherein the first and second gate separation patterns are spaced apart from each other with the MOSFET region therebetween and the second gate separation pattern is adjacent to the MOSFET region when viewed from a plan view, and
wherein the second gate separation pattern has a tensile strain when the MOSFET region is the PMOSFET region, and
wherein the second gate separation pattern has a compressive strain when the MOSFET region is the NMOSFET region.

9. The semiconductor device of claim 8, wherein
the MOSFET region includes a first MOSFET region and a second MOSFET region spaced apart from each other in the second direction;
the first MOSFET region corresponds to the PMOSFET region and the second MOSFET region corresponds to the NMOSFET region;
the first gate separation pattern is adjacent to the first MOSFET region and the second gate separation pattern is adjacent to the second MOSFET region; and
the first gate separation pattern has the tensile strain and the second gate separation pattern has the compressive strain.

10. The semiconductor device of claim 9, wherein
the device isolation layer extends between the first MOSFET region and the second MOSFET region, the semiconductor device further comprising:
a third gate separation pattern on the device isolation layer between the first MOSFET region and the second MOSFET region.

11. The semiconductor device of claim 10, wherein
a distance between the third gate separation pattern and the first MOSFET region is less than a distance between the third gate separation pattern and the second MOSFET region; and
the third gate separation pattern has a tensile strain.

12. The semiconductor device of claim 10, wherein
a distance between the third gate separation pattern and the second MOSFET region is less than a distance between the third gate separation pattern and the first MOSFET region; and
the third gate separation pattern has a compressive strain.

13. A semiconductor device comprising:
a substrate including at least one active pattern extending in a first direction;
a gate electrode intersecting the active pattern on the substrate, the gate electrode extending in a second direction intersecting the first direction;
source/drain regions on the active pattern at both sides of the gate electrode; and
a gate separation pattern adjacent to the active pattern when viewed from a plan view, the gate separation pattern dividing the gate electrode into segments spaced apart from each other in the second direction, and one of the active pattern and the gate separation pattern has a tensile strain and the other of the active pattern and the gate separation pattern has a compressive strain.

14. The semiconductor device of claim 13, wherein
the source/drain regions include P-type dopants;
the active pattern has the compressive strain; and
the gate separation pattern has the tensile strain.

15. The semiconductor device of claim 13, wherein
the source/drain regions include N-type dopants;
the active pattern has the tensile strain; and
the gate separation pattern has the compressive strain.

16. A semiconductor device comprising:
a substrate including at least one active pattern;
at least one gate electrode intersecting the active pattern on the substrate; and
an insulating pattern intersecting the gate electrode and adjacent to the active pattern when viewed from a plan view, one of the active pattern and the insulating pattern has a compressive strain and the other of the active pattern and the insulating pattern having a tensile strain.

17. The semiconductor device of claim 16, wherein
the active pattern has the compressive strain; and
the insulating pattern includes silicon oxide (SiO_2) and has the tensile strain.

18. The semiconductor device of claim 17, further comprising:
source/drain regions on the active pattern at both sides of the gate electrode, the source/drain regions including P-type dopants.

19. The semiconductor device of claim 16, wherein
the active pattern has the tensile strain; and
the insulating pattern includes silicon nitride (SiN) and has the compressive strain.

20. The semiconductor device of claim 19, further comprising:
source/drain regions on the active pattern at both sides of the gate electrode, the source/drain regions including N-type dopants.

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